a logic built-in self-test state machine; and

a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

19. The integrated circuit device of claim 17, wherein the built-in self-test controller further comprises a memory built-in self-test domain.

20. The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.

21. A method for performing a built-in self-test on an integrated circuit device, comprising:

externally resetting a built-in self-test controller including a logic built-in self-test engine;

performing a logic built-in self-test from the built-in self-test controller at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test; and

obtaining the results of the performed built-in self-test.

22. The method of claim 21, wherein resetting the built-in self-test controller includes initializing a multiple input signature register and a pattern generator.

23. The method of claim 21, wherein performing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the dual mode built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.

24. The method of claim 23, further comprising at least one of:

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

25. The method of claim 21, wherein externally resetting a built-in self-test controller includes resetting a built-in self-test controller including a memory built-in self-test engine and the method further comprises:

performing a memory built-in self-test from the built-in self-test controller; and

obtaining the results of the performed built-in self-test.

26. A method for testing an integrated circuit device, comprising:

interfacing the integrated circuit device with a tester;

externally resetting a built-in self-test controller including a logic built-in self-test engine;

performing a logic built-in self-test from the built-in self-test controller at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test; and

obtaining the results of the performed built-in self-test.

27. The method of claim 26, wherein resetting the built-in self-test controller includes initializing a multiple input signature register and a pattern generator.

28. The method of claim 26, wherein performing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the dual mode built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.

29. The method of claim 28, further comprising at least one of:

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

30. The method of claim 26, wherein externally resetting a built-in self-test controller includes resetting a built-in self-test controller including a memory built-in self-test engine and the method further comprises:

performing a memory built-in self-test from the built-in self-test controller; and

obtaining the results of the performed built-in self-test.

31. The method of claim 26, wherein obtaining the results includes reading at least one of a logic built-in self-test signature and a memory built-in self-test signature.

32. The method of claim 26, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.